IN THE CLAIMS:

No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as presented. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Previously Presented) A method for electrically coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate, comprising:

forming a hole having an inner surface from a first side of a semiconductor substrate to a second side of said semiconductor substrate;

forming an insulting layer from said first side to said second side of said semiconductor substrate on said inner surface in said hole; and

plating over said insulating layer on said inner surface of said semiconductor substrate to form a plated conductive element by forcing a plating solution from said first side of said semiconductor substrate and exiting said plating solution from said second side of said semiconductor substrate through said hole.

2. (Original) The method of claim 1, wherein forming said hole comprises at least one of ablating, mechanically drilling and chemically etching a portion of said semiconductor substrate from said first side to said second side.

3. (Original) The method of claim 1, further comprising loading said semiconductor substrate into a plating fixture, said semiconductor substrate and said plating fixture cooperatively directing flow of a plating material through said hole of said semiconductor substrate.

4. (Previously Presented) The method of claim 1, wherein said plating comprises electroplating over said insulating layer on said inner surface of said semiconductor substrate defined by said hole.

5. (Previously Presented) The method of claim 1, wherein said plating process comprises electroless plating over said insulating layer on said inner surface of said semiconductor substrate defined by said hole.

6. (Original) The method of claim 1, further comprising forming a conductive cap on at least one end of said plated conductive element.

7. (Original) The method of claim 1, further comprising etching one of said first and second sides of said substrate to expose at least one end portion of said plated conductive element.

8. (Original) The method of claim 7, further comprising forming a conductive cap over said at least one end portion of said plated conductive element.

9. (Previously Presented) The method of claim 1, wherein said hole is between approximately 50 microns and 700 microns in diameter.

10.-20. (Canceled)